FIG 1

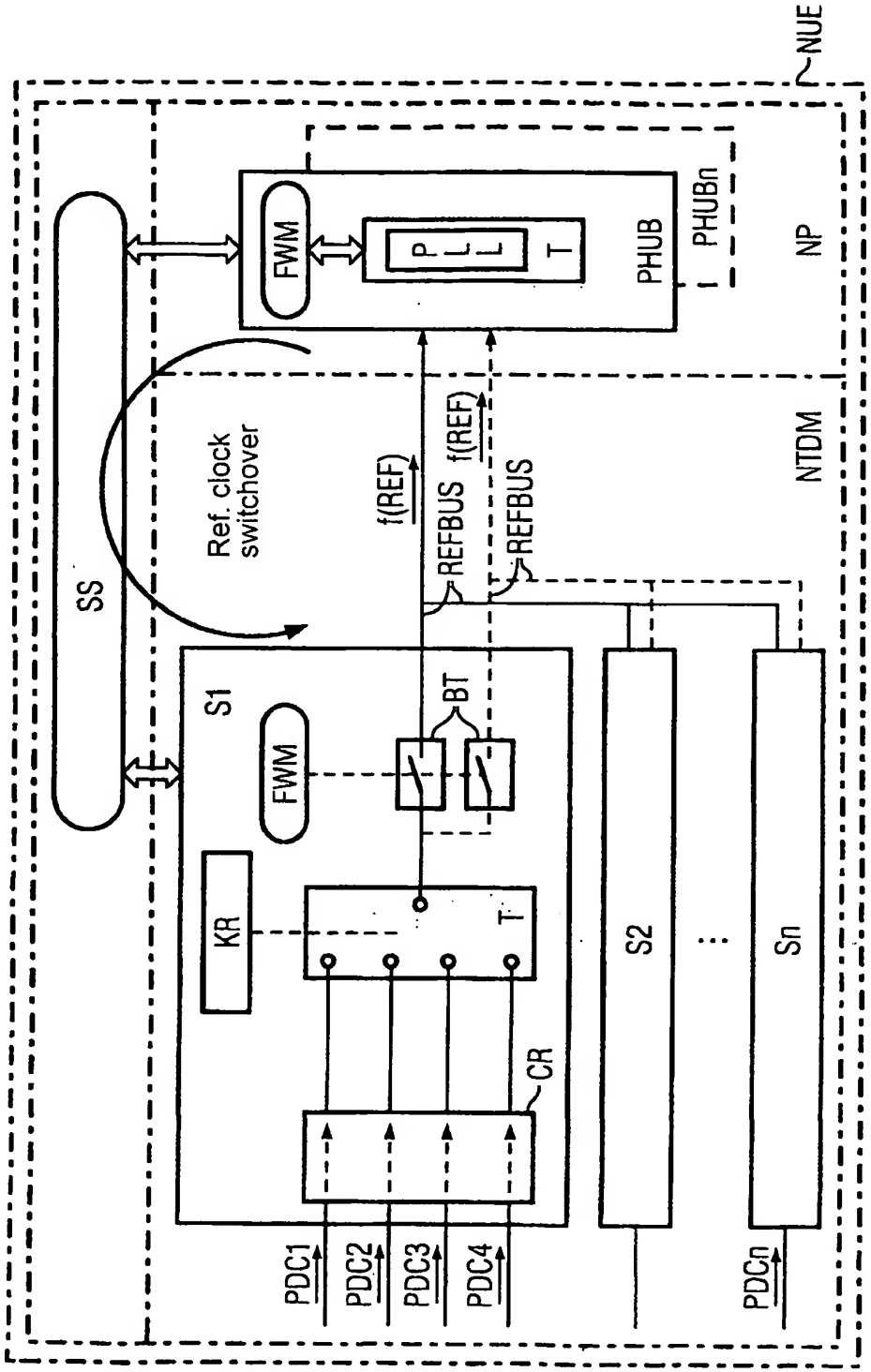
NUE
NP
PHUBn
PHUB
FWM
P
L
L
T
NTDM
Ref. clock switchover
f(REF)
REFBUS
f(REF)
REFBUS
SS
S1
FWM
BT
KR
T
CR
S2
Sn
PDC1
PDC2
PDC3
PDC4
PDCn

FIG 2

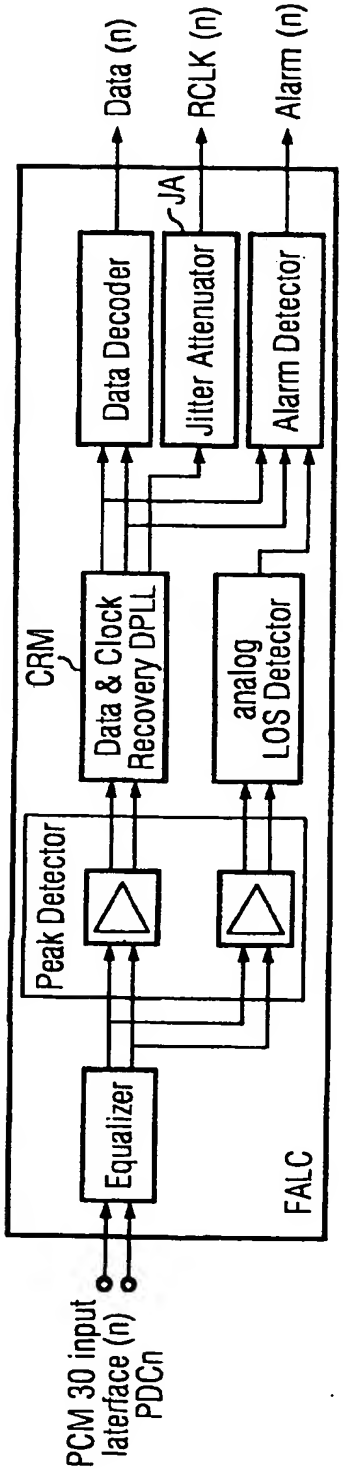
Data (n)
RCLK (n)
Alarm (n)
JA
Data Decoder
Jitter Attenuator
Alarm Detector
CRM
Data & Clock Recovery DPLL
analog LOS Detector
Peak Detector
Equalizer
FALC
PCM 30 input laterface (n) PDCn

FIG 8

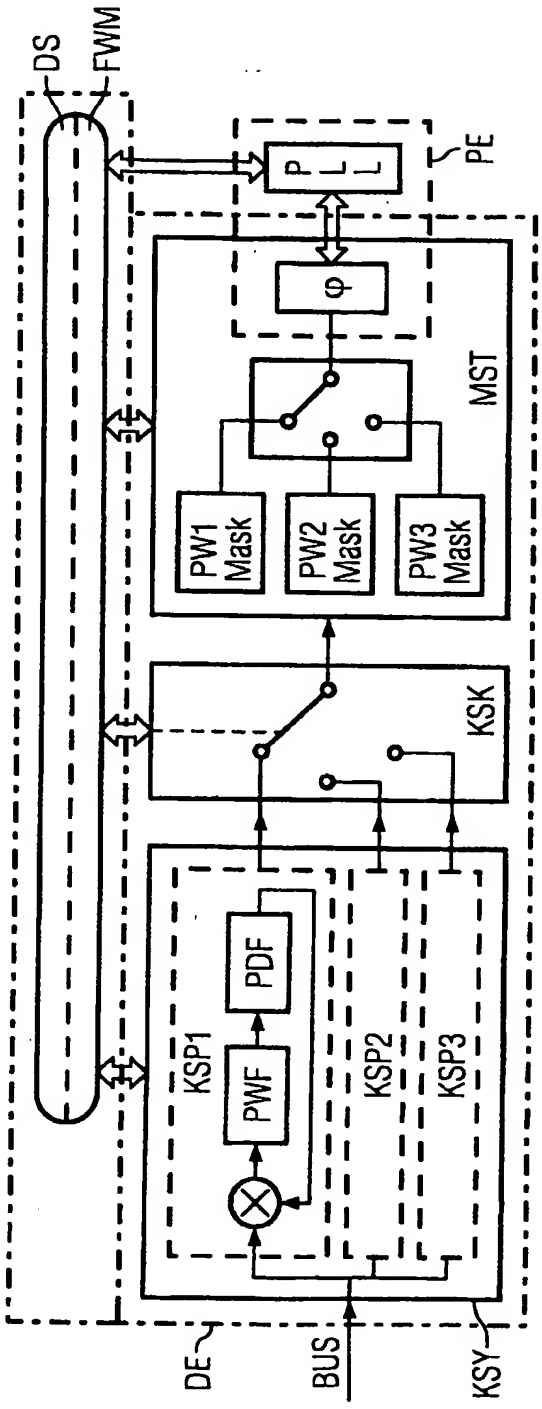
DS
FWM
P
L
L
PE
φ
MST
PW1 Mask
PW2 Mask
PW3 Mask
KSK
KSP1
PDF
PWF
KSP2
KSP3
DE
BUS
KSY

FIG 3

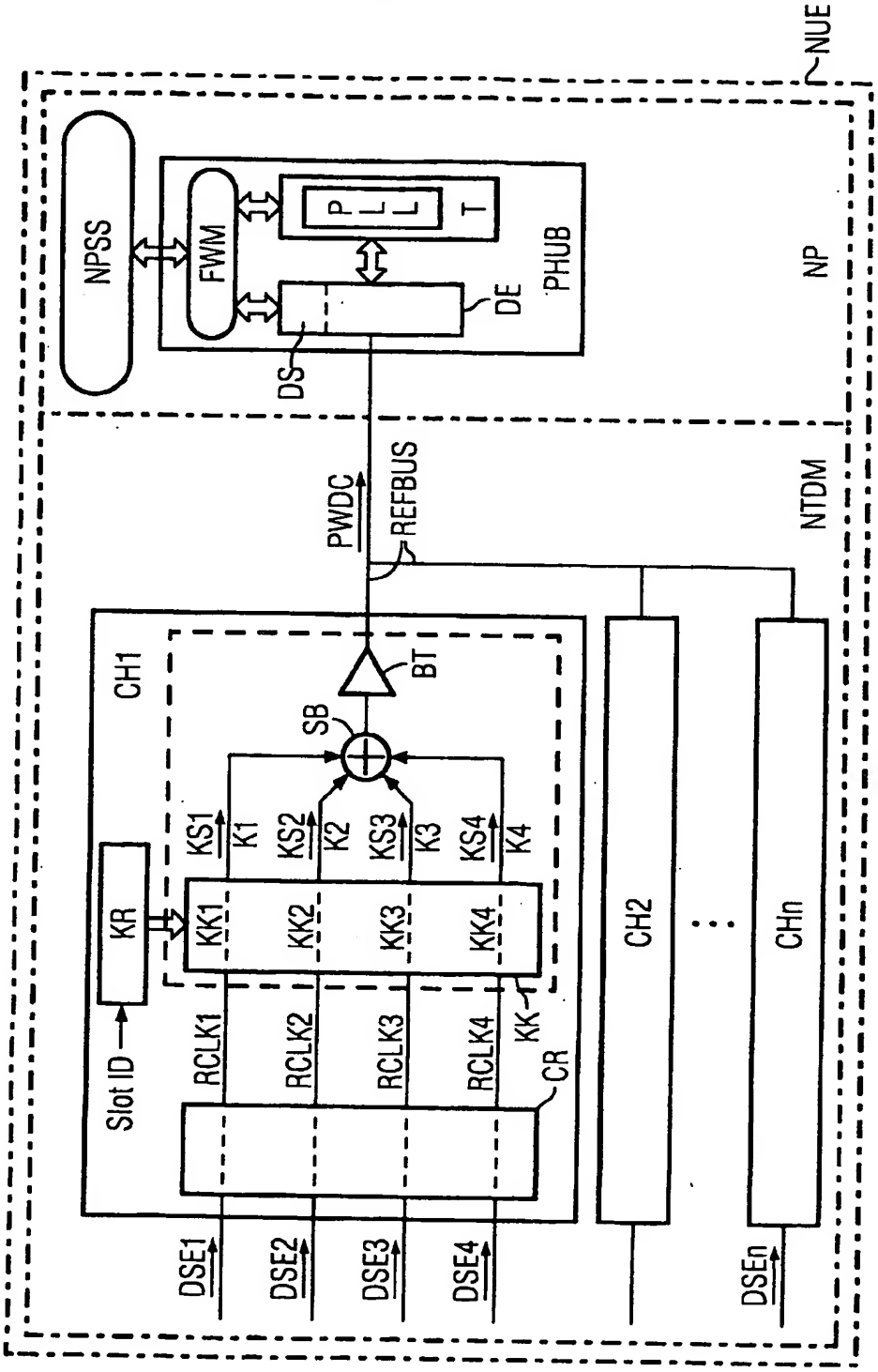
NUE
NP
NPSS
FWM
P
L
L
T
PHUB
DE
DS
PWDC
REFBUS
NTDM
CH1
BT
SB
KS1
K1
KS2
K2
KS3
K3
KS4
K4
KR
KK1
KK2
KK3
KK4
KK
CR
Slot ID
RCLK1
RCLK2
RCLK3
RCLK4
CH2
CHn
DSE1
DSE2
DSE3
DSE4
DSEn

FIG 4

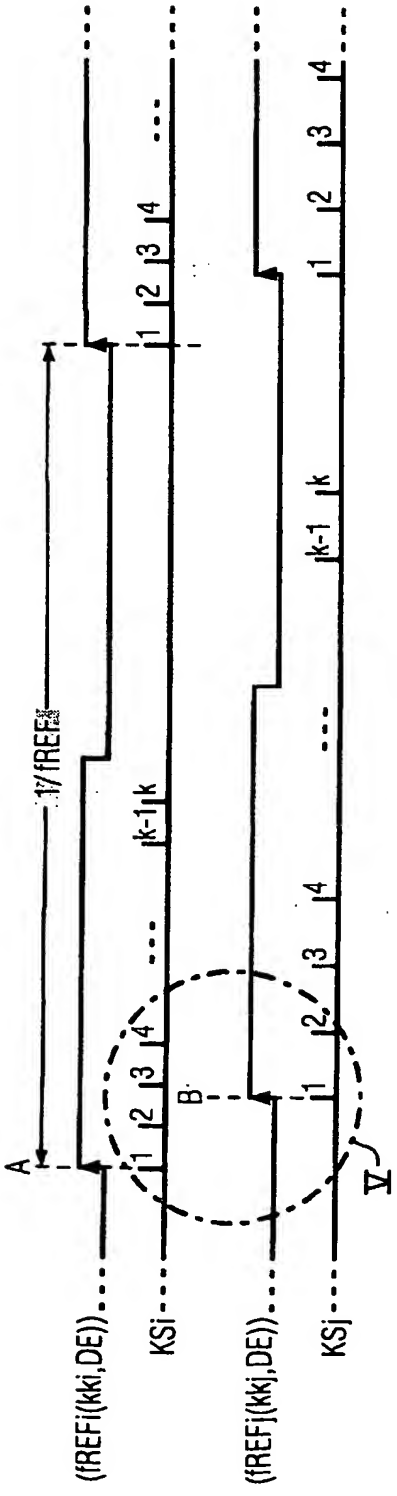
1/fREF
A
B
V
(fREFi(kki,DE))
KSi
(fREFj(kkj,DE))
KSj
1
2
3
4
k-1
k

FIG 5

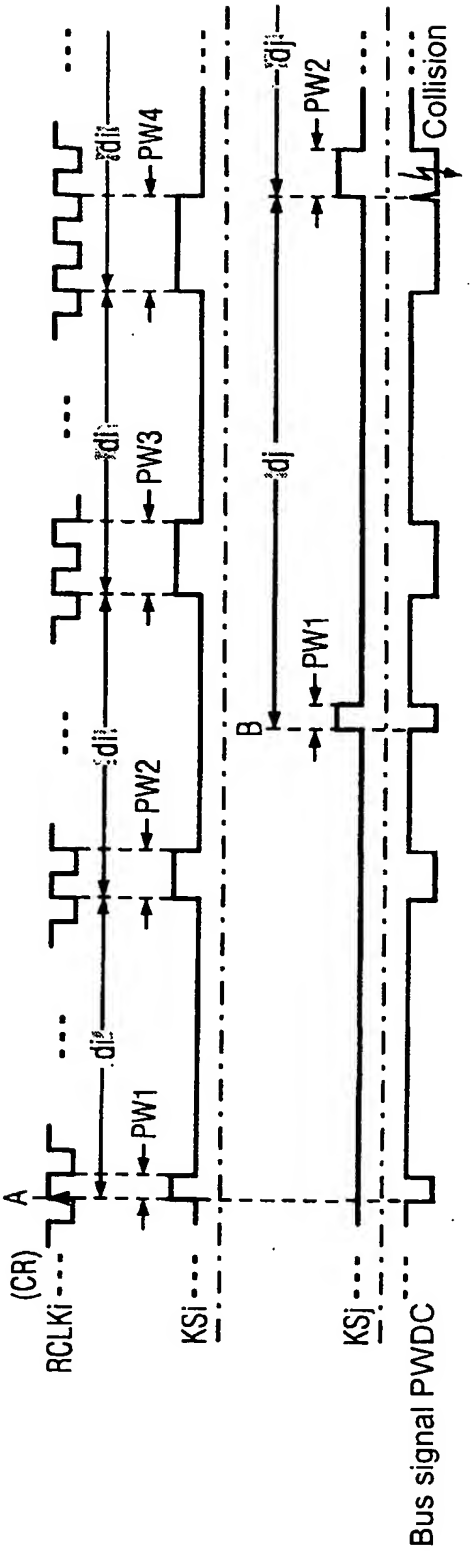
A
B
(CR)
RCLKi
KSi
KSj
Bus signal PWDC
di
dj
PW1
PW2
PW3
PW4
Collision

FIG 6

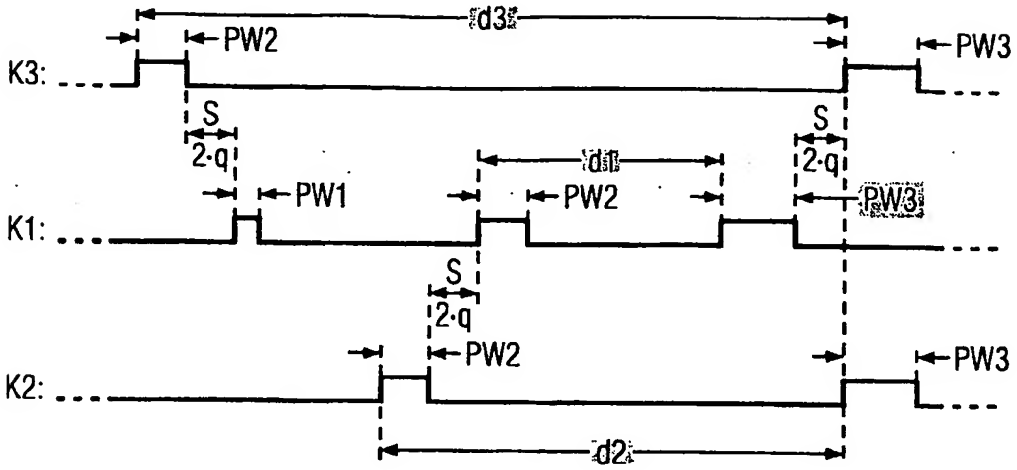
d3
PW2
PW3
K3:
S
2·q
d1
PW1
PW2
PW3
K1:
S
2·q
S
2·q
PW2
PW3
K2:
d2

FIG 7

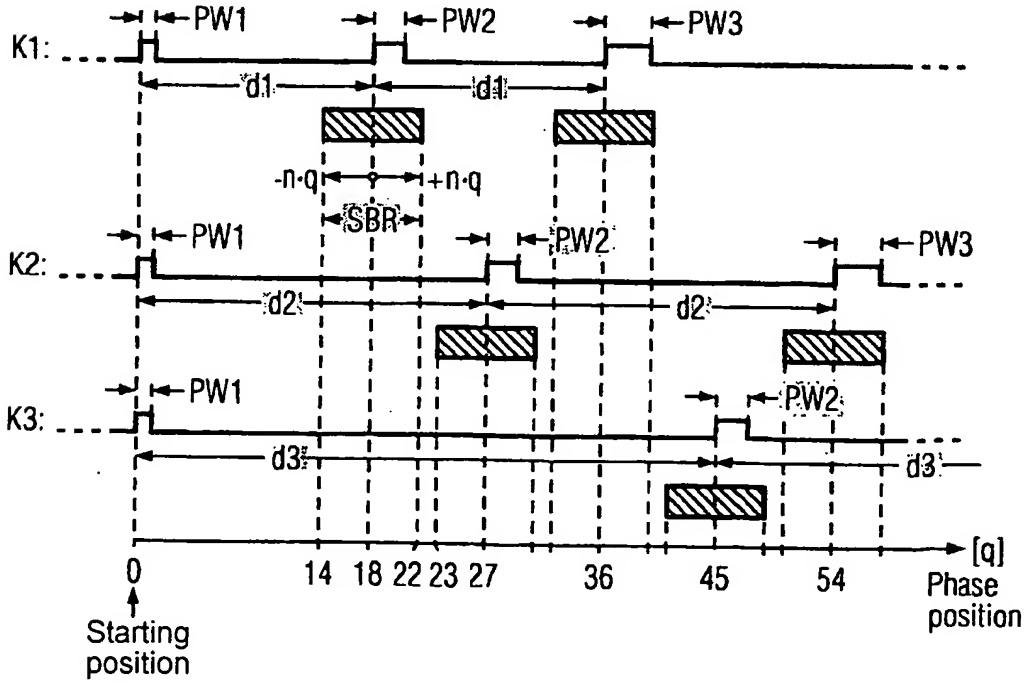
PW1
PW2
PW3
K1:
d1
d1
-n·q
+n·q
SBR
PW1
PW2
PW3
K2:
d2
d2
PW1
PW2
K3:
d3
d3
0
14 18 22 23 27
36
45
54
[q]
Phase position
Starting position

FIG 9

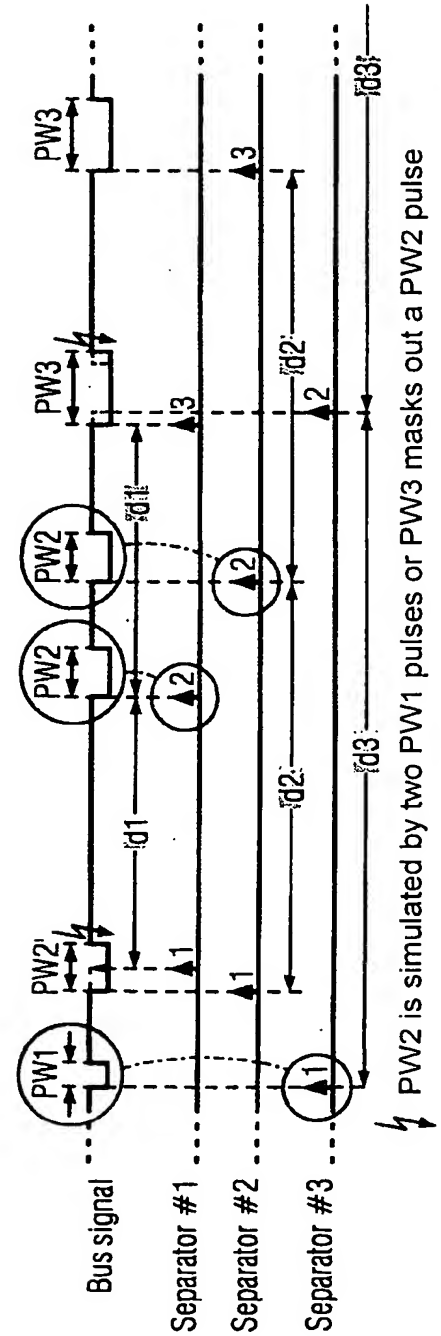
Bus signal
Separator #1
Separator #2
Separator #3
PW1
PW2'
PW2
PW3
td1
td2
td3
PW2 is simulated by two PW1 pulses or PW3 masks out a PW2 pulse

FIG 10

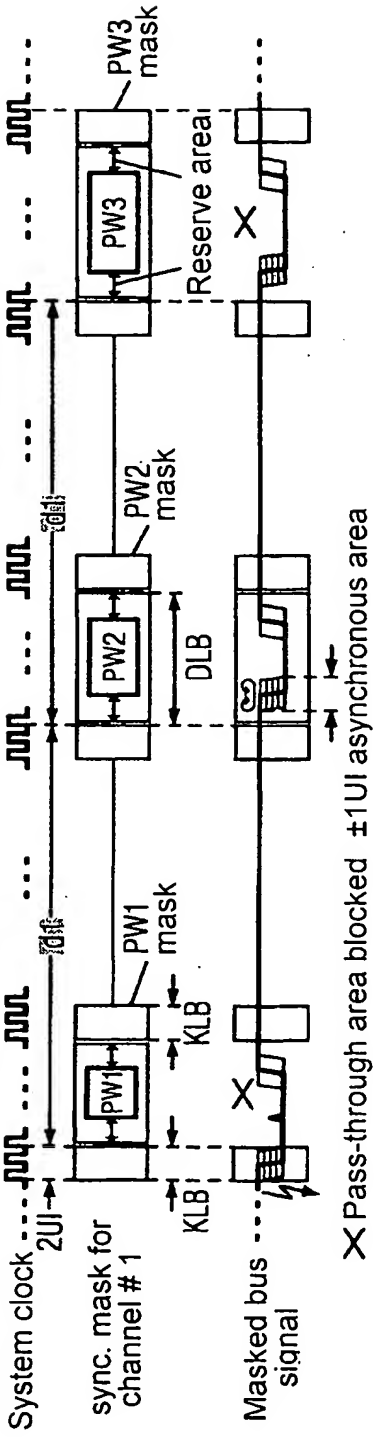
System clock
sync. mask for channel # 1
Masked bus signal
2UI
PW1 mask
PW2 mask
PW3 mask
KLB
DLB
Reserve area
Pass-through area blocked ±1UI asynchronous area

FIG 11

3-channel PWDC system

Pulse widths: PW1=q; PW2=2q; PW3=3q [n=4 for 2q safety margin]

Quantizing (q) = [61] ns Blocking area (n) = [4] Max. reference freq.= [118] kHz

d1 (distance) = [18] > 18 d2 (distance) = [27] > 27 d3 (distance) = [45] > 45

d1(-n·q...+n·q)= 14...22	d2(-n·q...+n·q)= 23...31	d3(-n·q...+n·q)= 41...49
2d1(-n·q...+n·q)= 32...40	2d2(-n·q...+n·q)= 50...58	2d3(-n·q...+n·q)= 86...94

opt. scheme →	1.	2.	4.
for gapless interleaving	3.	5.	6.

Pulse distance algorithm →
1) d1>=2(2n+1)
2) d2>=d1+(2n+1)
3) d3>=2d1+(2n+1)

FIG 12

4-channel PWDC system

Pulse widths : PW1=q; PW2=2q; PW3=3q; PW4=4q [n=5 for 2q safety margin]

Quantizing (q) = [61] ns Blocking area (n) = [5] Max. reference freq. = [52] kHz

d1 (distance) = [33] > 33 d2 (distance) = [44] > 44 d3 (distance) = [55] > 55 d4 (distance) = [77] > 77

d1(-n·q...+n·q)= 28...38	d2(-n·q...+n·q)= 39...49	d3(-n·q...+n·q)= 50...60	d4(-n·q...+n·q)= 72...82
2d1(-n·q...+n·q)= 61...71	2d2(-n·q...+n·q)= 83...93	2d3(-n·q...+n·q)=105...115	2d4(-n·q...+n·q)=149...159
3d1(-n·q...+n·q)= 94...104	3d2(-n·q...+n·q)=127...137	3d3(-n·q...+n·q)=160...170	3d4(-n·q...+n·q)=226...236

opt. scheme →	1.	2.	3.	5.
for gapless interleaving	4.	6.	8.	10.
	7.	9.	11.	12.

Pulse distance algorithm →
1) d1>=3(2n+1)
2) d2>=d1+(2n+1)
3) d3>=d2+(2n+1)
4) d4>=2d1+(2n+1)